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Carlynn F. Gould  
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3/18/02

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

Thomas G. Ference et al.

Serial No.: 09/261,328

Filed: March 3, 1999

For: **ULTRA-FINE CONTACT  
ALIGNMENT**

: Conf. No.: 7631

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Art Unit: 2814

Examiner: D. Graybill

Atty Docket: IBM - BU9-98-202  
CBLH- 21806/0059

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MAR 11 2002

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**RESPONSE AND AMENDMENT UNDER 37 CFR §1.111**

March 11, 2002

Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the Official Action dated December 11, the following amendments and remarks are submitted in connection with the above-identified application:

**IN THE SPECIFICATION:**

Please replace the paragraph starting at line 21, page 10 of the Specification and continuing through line 9, page 11, with the following replacement paragraph:

--The first solder bumps accomplish a rough self-alignment of two substrates. To achieve this, not only may the first solder bumps be larger, but they may have a composition such that they melt at a lower temperature than the contacts, if the contacts are made of solder. Examples of materials that may be utilized to form the contacts include 90:10-97:3 lead:tin solder. In other words, solder that is from about 90% lead and about 10% tin to about 97% lead and about 3%

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tin. On the other hand, the solder bumps may be formed from eutectic lead/tin solder having a composition of about 37% lead and about 63% tin, and having an eutectic temperature of about 183°C. Additionally, non-Pb-based solders may also be used for this invention.--

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**IN THE CLAIMS**

Please cancel claims 54 and 57 without prejudice or disclaimer as to the subject matter contained therein.

**Please amend claims 1 and 55 as follows:**

C2

1. (Twice Amended) A semiconductor structure for C4 interconnection of semiconductor devices, comprising:

- a first substrate;
- a second substrate joined to the first substrate;
- a plurality of C4 contacts between the first substrate and the second substrate; and
- a plurality of first solder bumps connected between the first substrate and the second substrate which substantially align the plurality of C4 contacts,

wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of C4 contacts,

wherein the plurality of C4 contacts are further aligned between the first and second substrates by a surface tension provided by a solder material which is in contact with each of the plurality of C4 contacts.

C3

55. (Amended) A semiconductor structure for C4 interconnection of semiconductor devices, comprising:

- a first substrate;
- a second substrate opposing the first substrate;
- a plurality of C4 contacts between the first substrate and the second substrate; and
- a plurality of first solder bumps connected between the first substrate and the second substrate which substantially align the plurality of C4 contacts,

wherein the plurality of first solder bumps are free of electrical connection with any of the plurality of C4 contacts,

C3  
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wherein the plurality of C4 contacts are further moved into an aligned position between the first and second substrates by a solder material positioned in tensioned contact with each of the plurality of C4 contacts.

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**Please add the following new claims:**

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C4

60. The semiconductor structure according to claim 1, wherein the plurality of C4 contacts comprise dendrites.

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61. The semiconductor structure according to claim 55, wherein the plurality of C4 contacts comprise dendrites.

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### REMARKS

Bearing in mind the comments of the Official Action and the discussion between the Examiner and Applicants' Representative during the interview conducted on March 8, 2002, the Application has been amended in a manner that is believed to place it in condition for allowance. An early indication of the same would be greatly appreciated.

Claims 1-25 and 54-61 are now pending in this application. Claims 1 and 55 are independent. Claims 1 and 55 have been amended, claims 54 and 57 have been canceled, and claims 60-61 have been added by this Amendment.

At the outset, applicant wishes to thank Primary Examiner Graybill for the courtesies extended during the personal interview held on March 8, 2002 with the undersigned attorney. The Examiner's professionalism and careful attention to the application on that occasion is sincerely appreciated.

Withdrawal of the rejection of claims 55-59 under 35 USC §112, second paragraph, as being indefinite, is requested. Independent claim 55 has been amended in a manner that is believed to overcome the basis for rejection.

Withdrawal of the rejection of claims 1, 3-6, 17, 18, 20, 25, 54-57, and 59 under 35 USC §102(b) as being anticipated by Nishiguchi et al. (USP 5,214,308) is requested.

Applicants note that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.<sup>1</sup> There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.<sup>2</sup> To properly anticipate a claim, the reference must teach every element of the claim.<sup>3</sup> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or

<sup>1</sup> *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).

<sup>2</sup> *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).

<sup>3</sup> See MPEP § 2131.

inherently described, in a single prior art reference".<sup>4</sup> "The identical invention must be shown in as complete detail as is contained in the ...claim."<sup>5</sup> In determining anticipation, no claim limitation may be ignored.<sup>6</sup> In view of the foregoing authority, the cited reference fails to anticipate independent claims 1 and 55, as amended.

Claim 1 has been amended to recite a semiconductor structure for C4 interconnection of semiconductor devices, which includes, among other features, "...a plurality of C4 contacts between the first substrate and the second substrate...wherein the plurality of C4 contacts are further aligned between the first and second substrates by a surface tension provided by a solder material which is in contact with each of the plurality of C4 contacts."

Somewhat similarly, independent claim 55 has been amended to recite a semiconductor structure for C4 interconnection of semiconductor devices, which includes, among other features, "...a plurality of C4 contacts between the first substrate and the second substrate...wherein the plurality of C4 contacts are further moved into an aligned position between the first and second substrates by a solder material positioned in tensioned contact with each of the plurality of C4 contacts."

The applied art, Nishiguchi et al. in particular, does not disclose, teach, or suggest these recited features.

By way of background, the present application, in a preferred embodiment, is concerned with providing a structure and method for joining two substrates in a semiconductor structure for "controlled collapse chip connection" (C4) interconnection of devices having self-aligning capabilities to ensure proper alignment of the two structures joined. The self-aligning aspects of Applicants' invention are brought about by using relatively "large" solder bumps to roughly, or initially align a plurality of C4 contacts between two substrates. Then, surface tension in wetted solder which is in contact with each of a plurality of C4 contacts is relied upon to finely align the tightly spaced C4 interconnects to a level, typically, within 10% of the solder bump diameter.

<sup>4</sup> *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

<sup>5</sup> *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The level of fine alignment of C4 interconnect achieved by Applicants' novel approach is submitted as not being achievable with conventional alignment techniques, such as are disclosed in the applied art, which rely upon physical force or external movement of the contacts to achieve alignment.

Consequently, within the arena of C4 technology, the present Application achieves an order of magnitude or more improvement in the number of C4 interconnects which are now possible to be joined. For example, as discussed in the Specification, the conventional limit for C4 interconnection technology, which has a C4 connection diameter of about 50mm, on a pitch of about 100mm, is, at most, about 10,000 C4 interconnects. This results in a chip having an area of about 1cm<sup>2</sup>. The structure and method of the present Application allows a much greater interconnect density, compared with current C4 technology, e.g., 100,000 interconnects per square centimeter, an order of magnitude or more increase, between the structures being joined.

For such an improved contact density, the contacts would have approximately, for example, a 15µm diameter, on a pitch of approximately 30µm. To achieve about 50% alignment of the C4 contacts, a 7.5µm alignment tolerance would be necessary from the initial alignment of the rough align solder bumps, i.e., the "larger" bumps. The large solder bumps have approximately a 10% alignment capability, allowing use of a solder bump having approximately a 75µm diameter, on a 150µm pitch. These limits on the large solder bumps are readily achievable with conventional component placement machines. The fine alignment achieved by the recited invention does not rely upon the machine placement accuracy, as long as the large solder bumps are placed within the above limits, for example. Surface tension acting on the C4 contacts is used to achieve the fine C4 interconnect alignment.

In contrast, Nishiguchi et al. is directed to a substrate for packaging a semiconductor device having a relatively large bump, which is received by a recess having an electrode terminal therein. The particular point of novelty of Nishiguchi et al. appears to be the use of a recessed electrode terminal as shown in Figs. 2-3, rather than merely a flat electrode terminal. The recessed electrode terminal is used for "coarse" positioning by physically moving the device,

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<sup>6</sup> *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

e.g., with a component placement machine, and then more precise positioning is accomplished by "merely lightly pushing the semiconductor device to the packaging substrate after coarse positioning to assure that the tops of the higher bump electrodes do not swell out of the recesses formed in the higher electrode terminals, the bump electrodes on the semiconductor device can be highly precisely positioned to the electrode terminals on the packaging substrate."<sup>7</sup>

By using the approach of Nishiguchi et al., the precision requirement for a positioning machine used to place the components in position for packaging was relaxed from  $\pm 10\mu\text{m}$  to  $\pm 50\mu\text{m}$ . With reference to Fig. 2 of Nishiguchi et al., a representative size of bump 2 formed on the semiconductor device 1 is indicated as being  $80\mu\text{m}$  in diameter, while electrode terminal 5 on substrate 3 has a diameter of  $100\mu\text{m}$ .

Thus, it appears clear that, even if Nishiguchi et al. discloses a C4 interconnection structure which anticipates applicants' invention, not a clear proposition given the level of integration and density present in the present application, Nishiguchi et al., at best, represents the conventionally achievable C4 approaches which rely upon external, mechanical force to push the contacts into alignment. Such conventional approaches are submitted as being unable to provide an interconnection density as in the present application, as described in Applicants' background section of the Specification, and as discussed above.

Accordingly, since the applied art does not disclose all the claim limitations discussed above, withdrawal of the rejection and allowance of amended claims 1 and 55 are requested.

As for dependent claims 2-6, 10-18, 20, and 25, these claims ultimately depend from independent claim 1, and are submitted as being allowable at least on that basis, as well as in their own right. Dependent claims 56-59, depending from independent claim 55, are likewise submitted as being allowable at least on the basis of the allowability of independent claim 55, as well as on their own merits.

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<sup>7</sup> See Nishiguchi et al., col. 1, line 63+.



Further, Applicants also respectfully request rejoinder and allowance of previously non-elected, dependent species claims 7-9, 19, and 21-24. The scope of independent claim 1 is submitted as still reading on the species represented by the dependent claims identified above.

Withdrawal of the rejection of claims 10-15 as being unpatentable over Nishiguchi et al. is requested.

The Official Action indicates that, although Nishiguchi et al. does not explicitly teach the particular dimensional limitations of Applicants' claims 10-15, it would have been an "obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because Applicants have not disclosed that the dimensions are for a particular unobvious purpose, produced an unexpected result, or are otherwise critical, and it appear *prima facie* that the process would possess utility using another dimension."<sup>8</sup> Applicants respectfully traverse this assertion.

Applicants disagree, as the specification discusses the necessary structure, dimensional relationships, and alignment methodology required to achieve the fine alignment necessary for improved C4 contact interconnection, particularly where much higher contact densities, compared to the conventional approach, of about 100,000 contacts/cm<sup>2</sup> are necessary. Such contact densities are desirable in (C4) technology, and achievable by the recited invention, as discussed above. The claim recitations have been amended to incorporate limitations in the preamble, and in the body of the independent claims, to clarify that the invention is directed to C4 interconnection structures. The necessary structure and alignment methodology to meet the stated dimensional objectives of the present application are submitted as not being taught or suggested by any of the cited or applied art.

The dimensional limitations disregarded by the Examiner are discussed, with the requisite specificity in the specification, at least at page 11, lines 11 through page 12, line 3. Thus, Applicants submit that the recited dimensional limitations are not a matter of obvious design

choice, because the structure and dimensional aspects of the recited invention have been disclosed in terms of a particular, non-obvious purpose, with the criticality of the dimensions related to the function, structure, and design objectives of the claimed invention, i.e., a semiconductor device for C4 interconnection of semiconductor devices.

In view of the above, reconsideration and allowance of claims 10-15 are requested.

Withdrawal of the rejection of claims 2 and 16 under 35 U.S.C. §103(a) as being unpatentable over Nishiguchi et al. in view of Lin et al. (USP 3,871,015) is requested.

Lin et al. is directed to a flip-chip module with non-uniform connector joints which extends the life of a chip substrate module, by increasing the ability of at least some of the connector joints to withstand shear stress, by ensuring that not all of the connector joints are identical on the same chip, in terms of either geometry or material composition. The Official Action offers Lin et al. as disclosing the use of two different solder materials, each having different melting points.

Even assuming that the references are properly combinable as suggested by the Examiner, an assumption with which Applicants do not agree due to the disparate nature of the technical problems solved by each of the references and the present application, Lin et al. does not make up for the previously identified deficiencies of Nishiguchi et al. In particular Lin et al. is at least deficient with respect to providing a teaching or suggestion of a semiconductor structure for C4 interconnection of semiconductor devices, which discloses, among other features, that "...the plurality of C4 contacts are further aligned between the first and second substrates by a surface tension provided by a solder material which is in contact with each of the plurality of C4 contacts", as recited in independent claim 1, as amended.

Accordingly, reconsideration and allowance of claims 2 and 16 are requested.

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<sup>8</sup> See Official Action, p. 8, ¶15.

New dependent claims 60-61, depending from independent claims 1 and 55, respectively, are submitted as further defining the claimed invention, and are patentable at least on the basis of their respective independent claims, as well as in their own right.

In view of the above amendments and remarks, reconsideration and allowance of pending claims 1-53, 55-56, and 58-61 in connection with the present application are respectfully requested.

Applicants believe that the present application is in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires clarification, the Examiner may contact the undersigned attorney so that this Application may continue to be expeditiously advanced.

Respectfully submitted,



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Enclosure: Specification after Amendment  
Claims after Amendment

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**Specification After Amendment****IN THE SPECIFICATION:**

Please replace the paragraph starting at line 21, page 10 of the Specification and continuing through line 9, page 11, with the following replacement paragraph:

--The first solder bumps accomplish a rough self-alignment of two substrates. To achieve this, not only may the first solder bumps be larger, but they may have a composition such that they melt at a lower temperature than the contacts, if the contacts are made of solder. Examples of materials that may be utilized to form the contacts include 90:10-97:3 lead:tin solder. In other words, solder that is from about 90% lead and about 10% tin to about 97% lead and about 3% [solder] tin. On the other hand, the solder bumps may be formed from eutectic lead/tin solder [have] having a composition of about 37% lead and about 63% tin, and having [a] an eutectic temperature of about [183°C] 183°C. Additionally, non-Pb-based solders may also be used for this invention.--

**Claims After Amendment**

Please amend claim 1 as follows:

1. (Twice Amended) A semiconductor structure for C4 interconnection of semiconductor devices, comprising:

- a first substrate;
- a second substrate joined to the first substrate;
- a plurality of C4 contacts between the first substrate and the second substrate; and
- a plurality of first solder bumps connected between the first substrate and the second substrate which substantially align the plurality of C4 contacts,

wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of C4 contacts,

wherein the plurality of C4 contacts are further aligned between the first and second substrates by a surface tension provided by a solder material which is in contact with each of the plurality of C4 contacts.

55. (Amended) A semiconductor structure for C4 interconnection of semiconductor devices, comprising:

- a first substrate;
- a second substrate opposing the first substrate;
- a plurality of C4 contacts between the first substrate and the second substrate; and
- a plurality of first solder bumps connected between the first substrate and the second substrate which substantially align the plurality of C4 contacts,

wherein the plurality of first solder bumps are free of electrical connection with any of the plurality of C4 contacts,

wherein the plurality of C4 contacts are further moved into an aligned position between the first and second substrates by a solder material positioned in tensioned contact with each of the plurality of C4 contacts.